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T Ivanov, S Ortiz, A Mortazawi, E Schlecht, J .. - Microwave and Guided Wave Letters, IEEE [see also IEEE ..., 1997 - ieeexplore.ieee.org

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C Branas, FJ Azcondo, S Bracho - Electronics Letters, 1999 - ieeexplore.ieee.org

... K., and WHITE, 5: '**Estimation** of average switching activity in combinational ... is the capacitor ratio of the LCC **circuit** and the maximum **power** delivered to ...

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P Vuillod, L Benini, G De Micheli - ... international symposium on Low **power** electronics and design, 1997 - portal.acm.org

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B Palethorpe, M Sumner, DWP Thomas - Harmonics and Quality of **Power**, 2000. Proceedings. Ninth ..., 2000 - ieeexplore.ieee.org

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1 Power estimation approach for SRAM-based FPGAs

Karlheinz Weiß, Carsten Oetker, Igor Katchan, Thorsten Steckstor, Wolfgang Rosenstiel
February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**
Publisher: ACM Press

Full text available: pdf(846.14 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the power consumption estimation for the novel Virtex architecture. Due to the fact that the XC4000 and the Virtex core architecture are very similar, we used the basic approaches for the XC4000-FPGAs power consumption estimation and extended that method for the new Virtex family. We determined an appropriate technology-dependent power factor Kp to calculate the power consumption on Virtex-chips, and developed a special benchmark test design to condu ...

2 Fault emulation: a new approach to fault grading

Kwang-Ting Cheng, Shi-Yu Huang, Wei-Jin Dai
December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Computer Society

Full text available: pdf(128.05 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In this paper, we propose a method of using an FPGA-based emulation system for fault grading. The real-time simulation capability of a hardware emulator could significantly improve the run-time of fault grading, which is one of the most resource-intensive tasks in the design process. A serial fault emulation algorithm is employed and enhanced by two speed-up techniques. First, a set of independent faults can be emulated in parallel. Second, simultaneous injection of multiple dependent faults is ...

3 Fast transient power and noise estimation for VLSI circuits

Wolfgang T. Eisenmann, Helmut E. Graeb
November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**
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